IN THE CLAIMS:

Please amend the claims in the application as follows:

1-10. (Canceled).

11. (Currently Amended) A method of forming a metal-insulator-metal capacitor and an associated semiconductor transistor having a metal gate, said method comprising:

forming a first metal layer adjacent a sacrificial gate structure;

removing said sacrificial gate structure;

forming an insulator over said first metal layer; and

~~removing a portion of said first metal layer from a gate region; and~~

forming a second metal layer over said insulator and in a void left by said removing of said sacrificial gate structure ~~said gate region~~,

wherein said second metal layer comprises a gate of said transistor and a plate of said ~~transistor~~ capacitor.

12. (Currently Amended) ~~The method in claim 11, further comprising~~ A method of forming a metal-insulator-metal capacitor and an associated semiconductor transistor having a metal gate, said method comprising:

forming sidewall spacers adjacent sacrificial gate structures;

forming a first metal layer, wherein said first metal layer is formed over said sidewall spacers;

forming an insulator over said first metal layer;

removing a portion of said first metal layer from a gate region; and

forming a second metal layer over said insulator and in said gate region, wherein said second metal layer comprises a gate of said transistor and a plate of said capacitor.

13. (Currently Amended) The method in claim ~~11~~ 12, further comprising, after said forming of said sidewall spacers, doping source and drain regions in said substrate.

14. (Currently Amended) ~~The method in claim 11, further comprising~~ A method of forming a metal-insulator-metal capacitor and an associated semiconductor transistor having a metal gate, said method comprising:

forming a first metal layer;

planarizing said first metal layer;

forming an insulator over said first metal layer;

removing a portion of said first metal layer from a gate region; and

forming a second metal layer over said insulator and in said gate region,

wherein said second metal layer comprises a gate of said transistor and a plate of said capacitor.

15. (Original) The method in claim 14, wherein said planarizing of said first metal layer reduces voids and surface irregularities in said second metal layer.

16. (Canceled).

17. (Currently Amended) The method in claim 11 ~~16~~, wherein said insulator comprises both a capacitor insulator and a gate insulator.

18. (Original) The method in claim 11, wherein said plate comprises an upper plate of said capacitor.

19. (Currently Amended) A method of forming a metal-insulator-metal capacitor and an associated semiconductor transistor having a metal gate, said method comprising:

patterning sacrificial gate structures over a substrate;

forming sidewall spacers adjacent said sacrificial gate structures;

forming a first metal layer adjacent said sidewall spacers;

planarizing said first metal layer;

removing said sacrificial gate structures;

forming an insulator over said first metal layer;

removing a portion of said first metal layer from a gate region; and

forming a second metal layer over said insulator and in said gate region,

wherein said second metal layer comprises a gate of said transistor and a plate of said ~~transistor~~ capacitor.

20. (Original) The method in claim 19, wherein said planarizing of said first metal layer reduces voids and surface irregularities in said second metal layer.

21. (Original) The method in claim 19, wherein said insulator comprises both a capacitor insulator and a gate insulator.

22. (Original) The method in claim 19, further comprising, after said forming of said sidewall spacers, doping source and drain regions in said substrate.

23. (Original) The method in claim 21, wherein said plate comprises an upper plate of said capacitor.